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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,550	12/05/2003	Ming-Dou Ker	6811954-15U1	8001

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AKIN GUMP STRAUSS HAUER & FELD L.L.P.
ONE COMMERCE SQUARE
2005 MARKET STREET, SUITE 2200
PHILADELPHIA, PA 19103

EXAMINER	
NGUYEN, DAO H	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,550	KER ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 26-31* is/are rejected.

7)☒ Claim(s) *16-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0704*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communications dated 12/05/2003 to 09/28/2005.

Claims 1-31 are active in this application.

Applicant made a provisional election without traverse to prosecute the invention of Group I, claims 1-31, drawn to semiconductor devices, in the Response to Restriction Requirement filed 09/28/2005

Claim(s) 32-36 have been cancelled.

Applicant has the right to file a divisional application covering the subject matter of the non-elected/cancelled claims.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 07/07/2004. The references cited on the PTOL 1449 form have been considered.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

This application claims the benefit of the provisional application no. 60/487,581 filed 07/17/2003.

Specification

3. The specification is objected to for the following reason:

In the specification, page 10, lines 5-6, the reference numbers "316" should be changed to –318-- because the P^+ region is priorly referred to by reference number 318. Appropriate correction(s) is/are required.

The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. The claim is objected to for the following reasons:

In claim 16, line 4, a word "well" should be inserted between words "first" and "formed" to correct the typo error;

Similarly, in claim 19, a word "doped" should be inserted between words "third" and "region".

Appropriate correction(s) is/are required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claim(s) 1-15, and 26-31 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,566,715 to Ker et al.

Regarding claim 1, Ker discloses a semiconductor device suitable for applications in an electrostatic discharge (ESD) protection circuit, as shown in figs. 5b, 6, 9, and 11, comprising:

a semiconductor substrate 30;

a first well 44 formed in the substrate 30;

a second well 32 formed in the substrate 30; and

a first doped region 36 formed in the second well 32, wherein the first well 44, the second well 32, and the first doped region 36 collectively form a parasitic bipolar junction transistor (BJT), and wherein the first well is the collector of the BJT, the second well is the base of the BJT, and the first doped region is the emitter of the BJT. See also col. 4, lines 6-64; and col. 6, line 60 to col. 7, line 13.

Regarding claim 2, Ker discloses the semiconductor device wherein the first well 44 is n-type, the second well 32 is p-type, the first doped region 36 is n-type, and the parasitic BJT is an NPN BJT. See fig. 5b.

Regarding claim 3, Ker discloses the device comprising all claimed limitations. See col. 6, line 60 to col. 7, line 13.

Regarding claim 4, Ker discloses the semiconductor device further comprising a second doped region 38 formed in the first well 44; and a third doped region 40 formed in the substrate 30, wherein the second doped region 38 and the first well 44 are of a same type of conductivity (n-type), and the second doped region 38 is a contact to the first well 44, and wherein the third doped region 40 and the second well 32 are of a same type of conductivity (p-type), and the third doped region 40 is a contact to the second well 32. See fig. 5b.

Regarding claim 5, Ker discloses the semiconductor device further comprising an ESD detection circuit 62, wherein the first doped region is connectable to a power supply, wherein the second doped region is connectable to a contact pad for receiving an ESD, and wherein the third doped region is connectable to the ESD detection circuit coupled to the contact pad for detecting the ESD. See figs. 5-6 and col. 4, line 51 to col. 7, line 9.

Regarding claim 6, Ker discloses the semiconductor device wherein the ESD detection circuit 62 provides a trigger current to the third doped region in an ESD event, and wherein the trigger current triggers the parasitic BJT to conduct the ESD current from the second doped region to the first doped region or from the first doped region to the second doped region. See col. 4, line 51 to col. 7, line 9.

Regarding claims 7, 8, Ker discloses the semiconductor device comprising all claimed limitations. See figs. 5b, 6, 9, 11, and col. 4, line 51 to col. 7, line 9.

Regarding claim 9, Ker discloses the semiconductor device further comprising a fourth doped region 46 formed in the second well 32, wherein the fourth doped region 46 and the second well are of a same type of conductivity (p-type), wherein the fourth doped region is also a contact to the second well, wherein the third doped region 40 and the fourth doped region 46 are spaced apart from each other, and wherein the fourth doped region is connectable to the power supply. See figs. 5b, 6, 9, 11, and col. 4, line 51 to col. 7, line 9.

Regarding claim 10, Ker discloses the semiconductor device further comprising a second doped region 38 formed in the first well 44; a third doped region 40 formed in the substrate 32; and a fourth doped region 46 formed in the second well, wherein the first, second, third, and fourth doped regions 36/38/40/46 respectively are electrically

isolated from each other by a plurality of isolation regions 42. See figs. 5b; and col. 4, lines 10-34; and col. 7, lines 10-25.

Regarding claims 11, and 12, Ker discloses the semiconductor device wherein the isolation regions are shallow trench isolations (STIs), or local oxidation of silicon (LOCOS) regions. See figs. 5b; and col. 4, lines 10-34; and col. 7, lines 10-25.

Regarding claims 13-14, Ker discloses the semiconductor device comprising all claimed limitations. See figs. 5b, 6, 9, 11, and col. 4, line 10 to col. 7, line 25.

Regarding claim 15, Ker discloses the semiconductor device further comprising a second doped region 38 for receiving a trigger current or a trigger voltage in an ESD event, wherein a portion of the second doped region is formed in the first well 44, and another portion of the second doped region is formed in the second well 32, and wherein the trigger current or the trigger voltage triggers the BJT to discharge the ESD in the ESD event. See fig. 5b and col. 4, line 51 to col. 7, line 9.

Regarding claim 26, Ker discloses a semiconductor device suitable for applications in an electrostatic discharge (ESD) protection circuit, as shown in figs. 5b, 6, 9, 11, comprising:

a semiconductor substrate 30;

a first well 44 (the left well) formed in the substrate 30;

a second well 32 formed in the substrate;

a third well 44 (the right well) formed in the substrate 30;

a first doped region 36 (the left doped region) formed in the second well 32; and

a second doped region 36 (the right doped region) formed in the second well 32, wherein the first well 44, the second well 32, and the first doped region 36 collectively form a first parasitic bipolar junction transistor (BJT), and the second well 32, the third well 44, and the second doped region 36 collectively form a second parasitic BJT, and wherein the first well is the emitter of the first BJT, the third well is the emitter of the second BJT, the second well is the base of both of the first and the second BJTs, the first doped region is the collector the first BJT, and the second doped region is the collector of the second BJT. See also col. 4, line 10 to col. 7, line 25.

Regarding claim 27, Ker discloses the semiconductor device further comprising a third doped region 38 formed in the substrate, wherein the third doped region 40 is a contact to the first well 44 (on the left);

a fourth doped region 40 formed in the second well 32; and

a fifth doped region 38 (the right doped region 38) formed in the substrate 32, wherein the fifth doped region 38 is a contact to the third well 44, wherein the first and second doped regions 36 are connectable to a contact pad for receiving an ESD in an ESD event, the third and fifth doped regions 38 are connectable to a power supply, and the fourth doped 40 region is connectable to an ESD detection circuit, wherein the ESD

detection circuit is coupled to the contact pad for detecting the ESD. See figs. 5b, 6, 9, 11; and col. 4, line 51 to col. 7, line 9.

Regarding claim 28, Ker discloses the semiconductor device wherein a portion of the third (left) doped region 38 is formed in the first well 44 (left well), and another portion of the third doped region 38 is formed in the second well 32, and wherein a portion of the fifth (right) doped region 38 is formed in the second well 32, and another portion of the fifth doped region is formed in the third well 44 (right well). See fig. 5b.

Regarding claim 29, Ker discloses the semiconductor device wherein the ESD detection circuit triggers the first and second BJTs to conduct the ESD current from the first and second doped regions to the third and fifth doped regions, respectively, or from the third and fifth doped regions to the first and second doped regions, respectively. See figs. 5b, 6, 9, 11; and col. 4, line 51 to col. 7, line 9.

Regarding claim 30, Ker discloses the semiconductor device wherein the first (left) doped region 36, the second (right) doped region 36, the third (left) doped region 38, the fourth doped region 40, and the fifth (right) doped region 38 are isolated from each other by a plurality of gate structures 34, wherein a first gate structure is formed between the first and third doped regions, and the first gate structure, the first doped region, the third doped region, and the second well form a first MOS transistor, wherein a second gate structure is formed between the second and fifth doped regions, and

the second gate structure, the second doped region, the fifth doped region, and the second well form a second MOS transistor. See figs. 5b, 6, 9, 11; and col. 4, line 51 to col. 7, line 9.

Regarding claim 31, Ker discloses the semiconductor device wherein the first and the second gates 34 are both connectable to the ESD detection circuit to trigger the first and second BJTs to discharge the ESD current in an ESD event. See figs. 6, 9, 11; and col. 4, line 51 to col. 7, line 9.

Allowable Subject Matter

7. Claim(s) 16-25 are objected to for minor errors as set forth above, but would be allowable if rewritten to correct such errors, since the prior art of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed semiconductor device comprising (in addition to the other limitations in the claim) a first well, a second well, and a first doped region collectively form a first parasitic bipolar junction transistor (BJT); and the second well, a third well, and the first doped region collectively form a second parasitic BJT; wherein the first well is the collector of the first BJT, the third well is the collector of the second BJT, the second well is the base of both of the first and the second BJTs, and the first doped region is the emitter of both of the first and the second BJTs.

Conclusion

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
October 14, 2005